Claims

1. An integrated circuit including a field plated resistor, comprising:

a resistor formed in a substrate, the resistor having first and second contact regions:

a fist layer of insulative material over the resistor, the first layer of insulative material having a window therethrough to the first contact region;

a layer of doped polysilicon over the first layer of insulative material to define a field plate over the resistor, the polysilicon filling the window and making contact with the first contact region of the resistor, the field plate extending over the resistor body to proximate the second contact region;

a second layer of insulative material over the resistor, a portion of the second layer of insulative material covering the field plate, the second layer of insulative material having a first window therethrough to the field plate and a second window therethrough to the second contact region;

metal conductors extending over the polysilicon field plate, the conductors formed in the same layer of metal as forms contacts to the first and second contact regions of the resistor.

2. The integrated circuit as recited in claim 1, wherein the first insulative material is an oxide.

3. The integrated circuit as recited in claim 1, wherein the second insulative material is an oxide.

4. The integrated circuit as recited in claim 1, further comprising:

an insulative spacer formed around the field plate.

5. The integrated circuit as recited in claim 1, further comprising:

an enhanced contact region formed at a polysilicon-substrate interface in the window of the first layer of insulative material.

6. The integrated circuit as recited in claim 1, further comprising:

a first barrier layer formed at a metal-polysilicon interface in the first window of the second layer of insulative material.

7. The integrated circuit as recited in claim 6, further comprising:

a second barrier layer formed at a metal-first barrier layer interface in the first window of the second layer of insulative material.

8. The integrated circuit as recited in claim 1, further comprising:

a first barrier layer formed at a metal-substrate interface in the second window of the second layer of insulative material.

9. The integrated circuit as recited in claim 8, further comprising:

a second barrier layer formed at a metal-first barrier layer interface in the second window of the second layer of insulative material.

10. An integrated circuit including a field plated resistor, comprising:

a resistor formed in a substrate, the resistor having first and second contact regions:

a fist layer of insulative material over the resistor, the first layer of insulative material having a window therethrough to the first contact region;

a layer of doped polysilicon over the first layer of insulative material to define a field plate over the resistor, the polysilicon filling the window and making contact with the first contact region of the resistor, the field plate extending over the resistor body to proximate the second contact region;

a second layer of insulative material over the resistor, a portion of the second layer of insulative material covering the field plate, the second layer of insulative material having a first window therethrough to the field plate and a second window therethrough to the second contact region;

metal conductors in a first layer of metal in the integrated circuit extending over the polysilicon field plate, the conductors formed in the same layer of metal as forms contacts to the first and second contact regions of the resistor.

11. The integrated circuit as recited in claim 10, wherein the first insulative material is an oxide.

12. The integrated circuit as recited in claim 10, wherein the second insulative material is an oxide.

13. The integrated circuit as recited in claim 10, further comprising:

an insulative spacer formed around the field plate.

14. The integrated circuit as recited in claim 10, further comprising:

an enhanced contact region formed at a polysilicon-substrate interface in the window of the first layer of insulative material.

15. The integrated circuit as recited in claim 10, further comprising:

a first barrier layer formed at a metal-polysilicon interface in the first window of the second layer of insulative material.

16. The integrated circuit as recited in claim 15, further comprising:

a second barrier layer formed at a metal-first barrier layer interface in the first window of the second layer of insulative material.

17. The integrated circuit as recited in claim 10, further comprising:

a first barrier layer formed at a metal-substrate interface in the second window of the second layer of insulative material.

18. The integrated circuit as recited in claim 17, further comprising:

a second barrier layer formed at a metal-first barrier layer interface in the second window of the second layer of insulative material.

19. A field plated resistor, comprising:

a resistor formed in a substrate, the resistor having first and second contact regions:

a fist layer of insulative material over the resistor, the first layer of insulative material having a window therethrough to the first contact region;

a layer of doped polysilicon over the first layer of insulative material to define a field plate over the resistor, the polysilicon filling the window and making contact with the first contact region of the resistor, the field plate extending over the resistor body to proximate the second contact region;

a second layer of insulative material over the resistor, a portion of the second layer of insulative material covering the field plate, the second layer of insulative material having a first window therethrough to the field plate and a second window therethrough to the second contact region;

metal conductors extending over the polysilicon field plate, the conductors formed in the same layer of metal as forms contacts to the first and second contact regions of the resistor.

20. The field plated resistor as recited in claim 19, wherein the first insulative material is an oxide.

21. The field plated resistor as recited in claim 19, wherein the second insulative material is an oxide.

22. The field plated resistor as recited in claim 19, further comprising:

an insulative spacer formed around the field plate.

23. The field plated resistor as recited in claim 19, further comprising:

an enhanced contact region formed at a polysilicon-substrate interface in the window of the first layer of insulative material.

24. The field plated resistor as recited in claim 19, further comprising:

a first barrier layer formed at a metal-polysilicon interface in the first window of the second layer of insulative material.

25. The field plated resistor as recited in claim 24, further comprising:

a second barrier layer formed at a metal-first barrier layer interface in the first window of the second layer of insulative material.

26. The field plated resistor as recited in claim 19, further comprising:

a first barrier layer formed at a metal-substrate interface in the second window of the second layer of insulative material.

27. The field plated resistor as recited in claim 26, further comprising:

a second barrier layer formed at a metal-first barrier layer interface in the second window of the second layer of insulative material.

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